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APPLICATION	NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/701,557	,	11/06/2003	Hiroshi Yamamoto	8038-1049	9561	
466	759	90 12/28/2005		EXAMINER		
YOUNG	G & TH	IOMPSON	NGUYEN, HIEP			
745 SOU 2ND FL		RD STREET	ART UNIT	PAPER NUMBER		
ARLING	GTON,	VA 22202	2816	<u> </u>		
				DATE MAILED: 12/28/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)	•
	10/701,557	YAMAMOTO, HIROSHI	
Office Action Summary	Examiner	Art Unit	
·	Hiep Nguyen	2816	
The MAILING DATE of this communication appeariod for Reply	opears on the cover sheet w	rith the correspondence address	
A SHORTENED STATUTORY PERIOD FOR REP WHICHEVER IS LONGER, FROM THE MAILING I - Extensions of time may be available under the provisions of 37 CFR 1 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory perior - Failure to reply within the set or extended period for reply will, by statu. Any reply received by the Office later than three months after the mail earned patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUN .136(a). In no event, however, may a d will apply and will expire SIX (6) MO tte, cause the application to become A	CATION. reply be timely filed NTHS from the mailing date of this communication. BANDONED (35 U.S.C. § 133).	
Status			•
1) Responsive to communication(s) filed on 24	October 2005.		
2a)⊠ This action is FINAL . 2b)□ Th	is action is non-final.		
3) Since this application is in condition for allow	•	•	
closed in accordance with the practice under	Ex parte Quayle, 1935 C.I	D. 11, 453 O.G. 213.	
Disposition of Claims			
4) Claim(s) 3-9 is/are pending in the application			
4a) Of the above claim(s) is/are withdrast 5) Claim(s) is/are allowed.	awn from consideration.		
6)⊠ Claim(s) <u>——</u> is/are allowed.			
7) Claim(s) is/are objected to.			
8) Claim(s) are subject to restriction and	or election requirement.		
Application Papers			
9) The specification is objected to by the Examir	ner.		
10) The drawing(s) filed on is/are: a) ac		by the Examiner.	
Applicant may not request that any objection to the	e drawing(s) be held in abeya	nce. See 37 CFR 1.85(a).	
Replacement drawing sheet(s) including the corre	ction is required if the drawing	g(s) is objected to. See 37 CFR 1.121(d).	
11)☐ The oath or declaration is objected to by the E	Examiner. Note the attache	d Office Action or form PTO-152.	
Priority under 35 U.S.C. § 119			
12) Acknowledgment is made of a claim for foreig a) All b) Some * c) None of:	n priority under 35 U.S.C.	§ 119(a)-(d) or (f).	
1. Certified copies of the priority documer	nts have been received.		
2. Certified copies of the priority documer	nts have been received in A	Application No	
Copies of the certified copies of the pri	ority documents have beer	received in this National Stage	
application from the International Bure	, , , , , , , , , , , , , , , , , , , ,		
* See the attached detailed Office action for a lis	st of the certified copies no	received.	
Attachment(s)			
1) Notice of References Cited (PTO-892)		Summary (PTO-413)	
 Notice of Draftsperson's Patent Drawing Review (PTO-948) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08 		s)/Mail Date Informal Patent Application (PTO-152)	
Paper No(s)/Mail Date	6) ☑ Other: <u>att</u>		

Application/Control Number: 10/701,557

Art Unit: 2816

DETAILED ACTION

This is responsive to the amendment filed on 10-24-05. Applicant's arguments with respect to references (USP. 4,695,748 and USP. 6,588,001) have been carefully considered but they are not deemed to be persuasive to overcome the references. Thus, the claims remained rejected under these above references. The rejection might change slightly for clarification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Elassaad et al. (US 2004/0257207A1) in view of Porterfield (US Pat. 6,588,001) and Kumamoto (US Pat. 4,695,748).

Regarding claim 3, figure 3 of Elassaad shows a semiconductor device comprising: a plurality of repeaters (Sopt), inserted in the transmission line to divide the signal transmission line into a plurality of divided signal lines. Figure 3 of Elassaad does not show that each repeater comprises two inverters and the first inverter is larger than the second inverter. However, it is old and well known for one of ordinary skill in the art that a repeater comprises two inverters (see Porterfield, US Pat. 6,588,001; Fig. 2, col.1, lines 55-67). Figure 1 of Kumamoto teaches a circuit having a repeater circuit including two inverters (6) and (9) where in, the first inverter (6) has a current-driven capacities made larger than the current-driven capacities of the second inverter (9). The first inverter (6) detects in input voltage (at node N1) and the second inverter (9) amplifies the detected input voltage (col. 5, lines 20-29). The repeater circuit (6,9) of Kumamoto provides a repeater that detects and amplifies a signal with precision and high speed (Abstract). Therefore, it would have been obvious for one of ordinary skill in the art to replace the repeaters of Elassaad with the repeater taught by

Application/Control Number: 10/701,557

Art Unit: 2816

Kumamoto for providing repeaters that can detect and amplify an input voltage precisely at high speed.

Regarding claim 4, it is inherent that the divided signal lines, the distances between the repeaters are longer than the distance between two inverters in the repeater cell.

Regarding claims 5 and 6, the combination of Elassaad, Porterfield and Kumamoto shows a branch comprising another repeater (B, see attached paper) that includes a repeater, taught by Kumamoto, including two inverters; the first inverter having a current driveability larger than a current driveability of said second inverter. The input signal applied to the first inverter (A) is a clock signal.

Regarding claim 7, figures 3 and 6 of Elassaad show that the signal line has wire capacitance (Cw). The wire capacitance causes wire delay that is at least 7 times that of the driver (paragraph [0112]). Thus, the signal line has a higher capacitance than an input capacitance of the repeater.

Regarding claim 8, figures 3 and 6 of Elassaad show a semiconductor device comprising: first and second functional blocks, not shown, connected via a signal transmission line; plurality of repeaters (A, B) in the transmission line that divide the signal transmission line into plural divided signal lines, each of the divided signal lines having a higher capacitance than an input capacitance of a respective one of said repeaters connected thereto (paragraph [0112]). Figure 3 of Elassaad does not show that each repeater comprises two inverters and the first inverter is larger than the second inverter. However, it is old and well known for one of ordinary skill in the art that a repeater comprises two inverters (see Porterfield, US Pat. 6,588,001; Fig. 2, col.1, lines 55-67). Figure 1 of Kumamoto teaches a circuit having a repeater circuit including two inverters (6) and (9) where in, the first inverter (6) has a current-driven capacities made larger than the current-driven capacities of the second inverter (9). The first inverter (6) detects in input voltage (at node N1) and the second inverter (9) amplifies the detected input voltage (col. 5, lines 20-29). The repeater circuit (6,9) of Kumamoto provides a repeater that detects and amplifies a signal with precision and high speed (Abstract). Therefore, it would have been obvious for one of ordinary skill in the art to replace the repeaters of Elassaad with the repeater taught by Kumamoto for providing repeaters that can detect an input voltage precisely at high speed.

Application/Control Number: 10/701,557

Art Unit: 2816

Regarding claim 9, figure 3 of Elassaad shows a semiconductor device comprising: a signal transmission line and a plurality of repeaters to divide the signal transmission line into a plurality of divided signal lines. Figure 3 of Elassaad does not show that each repeater comprises two inverters and the first inverter is larger than the second inverter. However, it is old and well known for one of ordinary skill in the art that a repeater comprises two inverters (see Porterfield, US Pat. 6,588,001; Fig. 2, col.1, lines 55-67). Figure 1 of Kumamoto teaches a circuit having a repeater circuit including two inverters (6) and (9) where in, the first inverter (6) has a current-driven capacities made larger than the current-driven capacities of the second inverter (9). The first inverter (6) detects in input voltage (at node N1) and the second inverter (9) amplifies the detected input voltage (col. 5, lines 20-29). The repeater circuit (6,9) of Kumamoto provides a repeater that detects and amplifies a signal with precision and high speed (Abstract). Therefore, it would have been obvious for one of ordinary skill in the art to replace the repeaters of Elassaad with the repeater taught by Kumamoto for providing repeaters that can detect an input voltage precisely at high speed.

Response to Arguments

On page 5 of the Remarks the Applicant argues that "ELASSAAD et al. and PORTERFIELD discuss repeaters but, as acknowledged in the Official Action, do not disclose that the first logic gate has a higher current driveability than that of the second logic gate". On page 6, the Applicant argues that "it is noted that KUMAMOTO is unrelated to repeater". In fact, figure 2 of Porterfield shows a repeater cell (200) basically comprises two inverters (220, 215) connected in series for receiving (detecting) and boosting an input signal (col. 1, lines 55-67). Figure 1 of Kumamoto shows a circuit comprising a repeater (6,9) for detecting an input voltage (at node (N1) and amplifying that detected voltage at high speed. The repeater (6,9) comprises a first inverter (6) that has a current driveability larger than the current driveability of the second inverter (9) (see col. 5, lines 20-19). Therefore, it would have been obvious for one of ordinary skill in the art to replace the repeaters of Elassaad with the repeater taught by Kumamoto for providing precise and high speed repeaters for the transmission line (see Abstract).

Art Unit: 2816

Conclusion

Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

12-21-05

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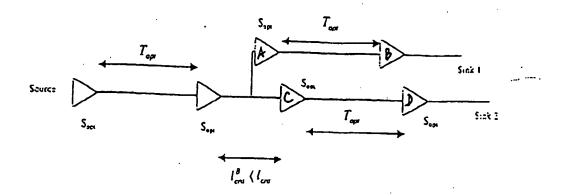


Fig. 3

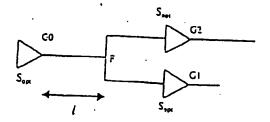


Fig. 4